ISE News

August 2004

Contents

Latest Edition

As Founder and CEO of ISE, I am proud to present the latest edition of our ISE News. Through this newsletter, the staff of ISE want to inform you about the status of our company and new developments that may interest you.

The excellent performance of ISE and its remarkable growth is a tribute to the quality of our software products and the excellent support, consulting, and engineering services of our staff. To accommodate the increasing demand, the ISE workforce has grown to nearly 100 staff members by the end of June 2004.

In this newsletter, we present application examples in several areas of high interest: strain-engineered devices for sub-100 nm CMOS; three-dimensional nonvolatile memory structures, their generation and meshing; the optimization of vertical-cavity surface-emitting lasers (VCSELs); and simulation aspects for modern CMOS image sensors. The VCSEL contribution, coauthored by one of our customers and one of our research consultants, is an example of the successful link between industry, academia, and ISE.

I trust that you will enjoy this newsletter and its contents. For further information, please visit our website.

With best regards,

W. Fichtner

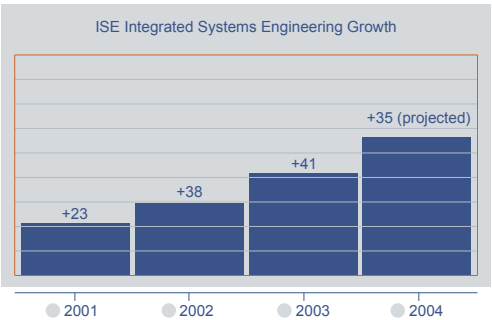
Wolfgang Fichtner

ISE on Strong Growth Path

Through considered planning and investment in key personnel and resources, ISE continues to expand its business and profitability.

After growing 38% in 2002 from 2001, we expanded our net sales by another 41% during the course of 2003 – the year of our tenth anniversary. This growth continued into 2004 where net sales are expected to increase by 35%. Consulting and customer engineering services have been the most strongly developing segment of ISE. This profitable growth is based on firm foundations. In addition to winning major new customers from around the globe, ISE is prospering because our long-standing customers repeatedly demonstrate their loyalty to ISE and their confidence in the ability of ISE to deliver results. We strive to maintain customer satisfaction through strong support and our continuing efforts to foster beneficial business relationships.

One of this year's highlights was the successful entry of ISE into the optoelectronics market. In addition to sales of ISE TCAD™ software to leading customers, we credibly established our optoelectronic calibration methodology in the industrial environment. Another highlight was the overwhelming demand for optimization of CMOS sensor devices.



TCAD for Manufacturing partnerships are continuing successfully. New products for this segment will be introduced in the second half of 2004. The quality of consulting and customer engineering services provided by ISE is largely due to our team of highly qualified, dedicated scientists and engineers – a real TCAD think tank. For us, customer-related projects are the best medium in which to transfer know-how to our customers.

With the steadily increasing number of customer-specific projects and the stream of new tools we will offer, we are confident that ISE will continue on this promising path for the foreseeable future.

Integrated Systems Engineering

Development, Modeling, and Optimization of Microelectronic Processes, Devices, Circuits, and Systems

Simulations of Strained Silicon CMOS Devices

Performance improvements for each new silicon CMOS technology generation have been driven mainly by geometric scaling, which implied increasing the channel doping concentration and vertical electrical field required to control short-channel effects. However, these two aspects of geometric scaling adversely affect carrier mobility due to impurity scattering and high-field saturation. Therefore, they diminish the improvements of the drive current. One way to counteract this is to enhance carrier mobility by changing the material properties in the channel. This is achieved by introducing strain.

Recently, Intel announced an approach [1] in which Si_xGe_{1-x} pockets were introduced into the source and drain of the PMOS device. These pockets create compressive stresses in the channel area. The NMOS device was fabricated using standard NMOS process flow but, at the end of the process flow, a highly tensile silicon-nitride capping layer was deposited, which covered the source, drain, and gate stack. This layer created tensile stresses in the channel. In both of these cases, stresses improved the performance of the transistor.

ISE TCAD™ has all the models required to perform process and device simulations of modern strained silicon and silicon-germanium devices. To demonstrate ISE TCAD capabilities for strained silicon, both process and device simulations for strained silicon CMOS devices are presented for a process similar to the technology presented by Intel [1].

FLOOPS-ISE™ features a special model for the simulation of strained silicon and silicon-germanium structures. In the model, the germanium content and boundary coordinate between strained and relaxed SiGe are given as input. Based on this information, which is continuously updated during simulation, FLOOPS-ISE automatically calculates the lattice mismatch and stress distribution in the structure. Therefore, this model captures the effect of change in material composition due to Ge diffusion and its effect on strain. These stresses are considered when mechanics equations are solved. The model is used to simulate the formation of a PMOS transistor.

In FLOOPS-ISE, germanium redistribution during high-temperature annealing is simulated as part of the germanium diffusion. The presence of germanium also influences the diffusion of all other species. FLOOPS-ISE takes this effect into account in three different ways. First, the band gap of silicon is lowered in the presence of germanium. Second, the introduction of germanium alters the thermodynamic equilibrium of the silicon matrix, that is, in the presence of germanium, the equilibrium concentrations of point defects change. Third, germanium forms pairs with boron. These GeB pairs are electrically active but not mobile.

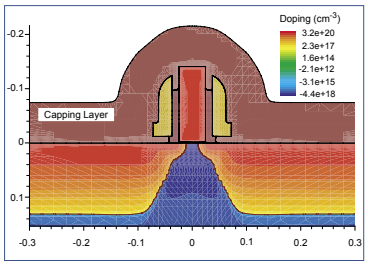


Figure 1: Doping distribution in strained-silicon NMOS transistor; distances are µm

All three aspects of the germanium influence on the diffusion of dopants are taken into account by default. In addition to these effects, the stresses modify the equilibrium state of the lattice. For example, compressive (negative) stress increases the equilibrium concentration of vacancies and decreases the equilibrium concentration of interstitials. FLOOPS-ISE automatically accounts for the influence of the altered point-defect concentration on the diffusion of dopants if a pair diffusion model is used.

By default, the stress evolution is computed at each step of the process simulation including oxidation steps based on the FLOOPS-ISE viscoelastic model. In particular, this model is used to compute the stress evolution in the NMOS transistor after the deposition of the highly tensile cap layer.

Device simulations were performed by DESSIS™. Two strain-specific models captured the influence of stress on carrier transport: the Egley strained-silicon mobility model and the Bir and Pikus model, which describes the dependence of the band gap on stress.

Given that the silicon-germanium pockets in the source and drain areas of the PMOS device lead to heterojunctions, DESSIS automatically accounts for the transport across this heterointerface.

NMOS Transistor

Figure 1 shows an overall view of the doping distribution in the strained-silicon NMOS transistor. To highlight the changes in stress distribution induced by the capping layer of the NMOS transistor, a control simulation was performed in which it was assumed that the deposited capping layer was grown relaxed and did not induce significant stresses.

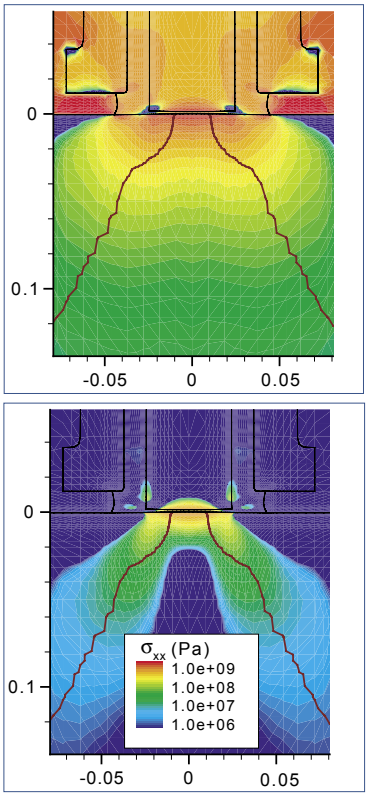


Figure 2: Comparison of XX component of stress tensor (σ_{xx}) between NMOS transistor with highly tensile capping layer (top) and device simulated with no-stress cap layer (bottom); distances are µm

Figure 2 shows a comparison between the devices simulated with a highly tensile capping layer and a relaxed capping layer. The comparison shows that stresses in the capping layer lead to tensile stress in the channel area.

The NMOS transistor with a highly tensile stress cap layer shows an improved saturation current I_{dsat} of about 16% compared to the device with the relaxed cap layer. The regular stress that originates from oxidation and other processing steps has a minor effect on electron transport.

In the technology discussed here, no new materials are introduced into the body of the transistor. Consequently, the threshold voltage and subthreshold currents for the strained and unstrained device are very similar. A relatively slight Vt shift of approximately 13 mV is a result of the strain-induced band-gap reduction.

PMOS Transistor

Figure 3 presents an overall view of the doping distribution in the strained-silicon PMOS transistor and the location of the silicon-germanium pockets. The pockets have a depth of 60 nm and are formed after the spacer formation, and before source and drain implant and anneal created by epitaxial growth of $Si_{0.83}Ge_{0.17}$. For comparison, a control PMOS structure without silicon-germanium pockets was simulated. Figure 4 shows the devices simulated with and without silicon-germanium pockets. The $Si_{0.83}Ge_{0.17}$ pockets induce compressive stresses in different areas of the structure, particularly the channel.

The presence of germanium and the stress in the structure alter the diffusion process for all dopants. A comparison of the final doping profiles in the two previously mentioned devices is shown in Figure 5. Significant difference in the final doping profiles can be seen. In the strained device, boron diffuses much more. The compressive stress in the channel area increases the concentration of interstitials. As boron mainly diffuses through interstitials, this leads to an effective increase in boron diffusivity. Further, at high boron concentrations, the presence of germanium increases boron diffusivity.

The stresses in the device contribute to an improvement of the saturation current I_{dsat} of about 16%.

For full details, visit the ISE website, www.ise.ch/appex/strain_si.

[1] T. Ghani et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," *IEDM Technical Digest*, Washington, D.C., USA, December 7–10, 2003.

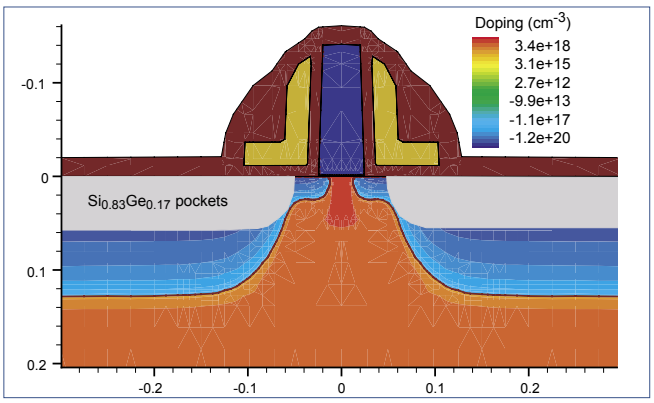


Figure 3: Doping distribution in strained-silicon PMOS transistor; gray regions show location of silicon-germanium pockets; distances are µm

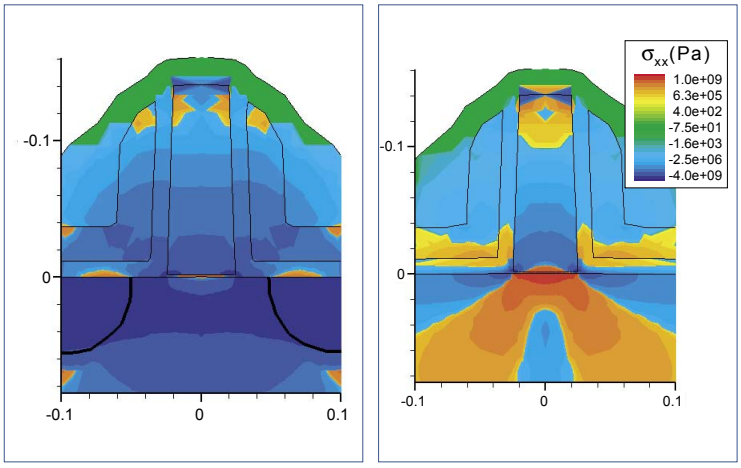


Figure 4: Comparison of XX component of stress tensor (σ_{xx}) between PMOS transistors with (left) and without (right) $Si_{0.83}Ge_{0.17}$ pockets

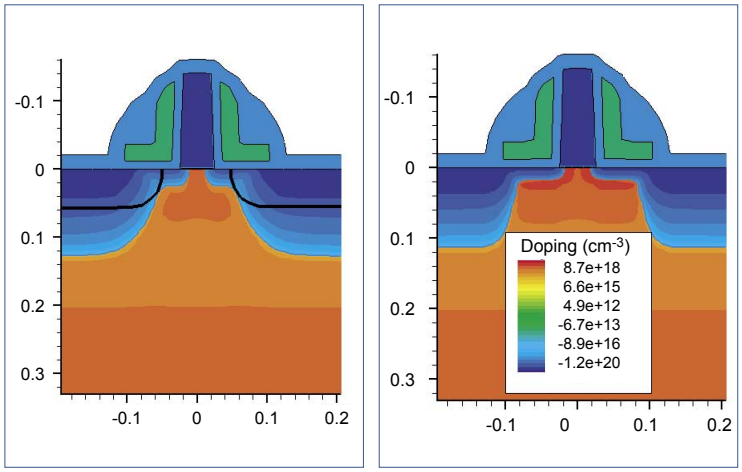


Figure 5: Comparison of final doping profiles in PMOS transistors with (left) and without (right) $Si_{0.83}Ge_{0.17}$ pockets

Geometry and Mesh Generation for Nonvolatile Memories

The simulation of nonvolatile memories (NVMs) such as electrically erasable programmable read-only memories (EEPROMs) has been very difficult or even impossible in many steps of the modeling, which comprised geometry generation, mesh generation, and device simulation.

As DEVISE™ becomes increasingly advanced, it is possible to create highly sophisticated geometries. For NVMs, it is important to model correctly the shape of the shallow trench isolation close to the channel region. In addition, the overetch at the gate oxide cannot be represented by planar faces only because the tunneling current largely depends on those shapes. The ACIS® library on which DEVISE is built offers many options to use arbitrary curves and faces, for example, circles and splines.

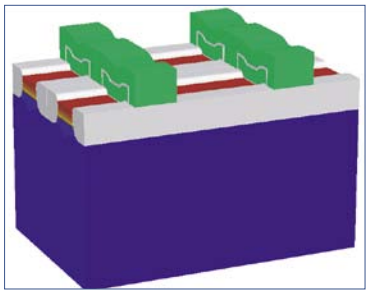


Figure 1: Four EEPROM cells created using DEVISE

Figures 1 and 2 show the result of generating multiple cells in DEVISE: Figure 1 shows the overall structure and Figure 2 shows the mesh generated by NOFFSET3D™. Due to symmetry, only one-eighth of the structure is constructed and, by repeated reflection operations, the complete structure is derived. The mesh can contain between 60 000 and 100 000 nodes depending on the simulation envisaged. NOFFSET3D is very helpful for NVMs since it can reliably generate meshes for rounded and non-axis-aligned structures. The construction of anisotropic layers in the channel regions helps to reduce the number of nodes.

In a second case, the dependency of the roundings of the oxide overetch on the Fowler–Nordheim tunneling current was studied. The scripting language of DEVISE makes it very easy to parameterize the structure and investigate the influence of the parameters. Figure 3 shows the rounded shapes applied in DEVISE and Figure 4 shows the tunneling current for erasing the cell in a DESSIS™ simulation. Since Fowler–Nordheim tunneling depends on the magnitude of the electric field in the oxide, it is expected that the current flows mainly – in this type of cell – at the oxide edge close to the source contact. Furthermore, the highest current is at both ends of this edge, close to the overetch rounding. This has been known for some time, but these effects can now be analyzed quantitatively with ISE TCAD™.

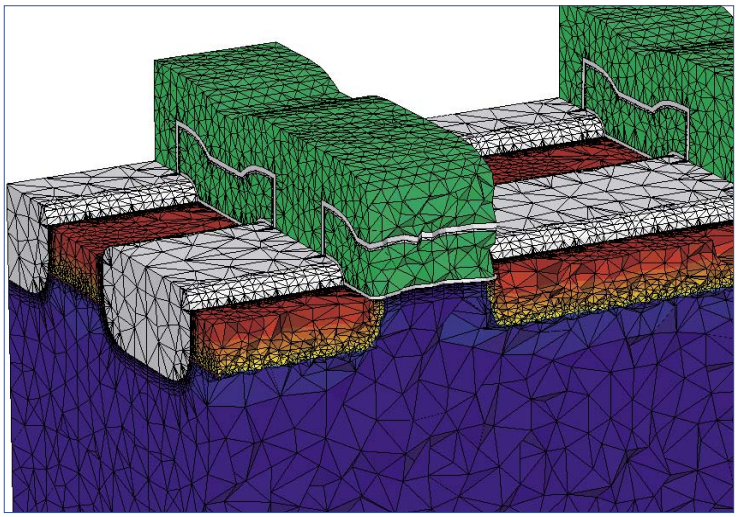


Figure 2: Mesh for simulation of cells; this inside view shows doping refinement at p-n junction and anisotropic layering in channel region

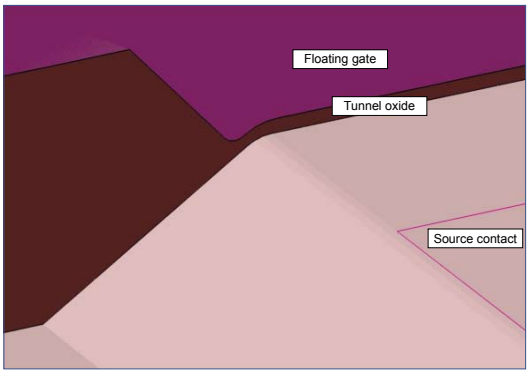


Figure 3: Rounded shapes are a more realistic model of overetch corners and are important for correctly modeling tunneling currents in NVMs

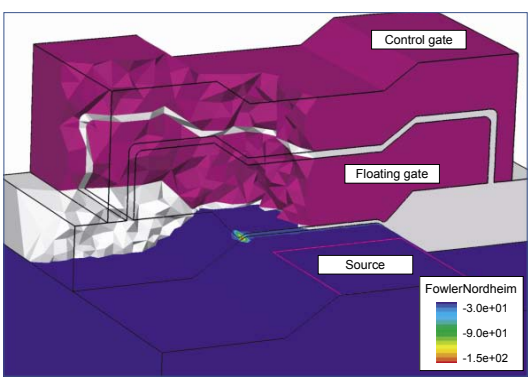


Figure 4: Simulating the tunneling current with DESSIS; the highest current (red) occurs at the oxide edge close to overetch corners; part of the top oxide and polysilicon layers are 'carved away' to display the current flow better

VCSEL Optimization in Industrial R&D

Paul Royo, Avalon Photonics Ltd and Matthias Streiff, ETH Zurich

This paper presents the design and implementation of a self-consistent electrothermo-optical device simulator for vertical-cavity surface-emitting lasers (VCSELs). The practical relevance of the implementation is demonstrated with the simulation of a realistic 850 nm single-mode VCSEL device produced by Avalon Photonics Ltd (www.avalon-photonics.com).

Introduction

With their small size and circular symmetry, VCSELs have emerged as an attractive alternative to conventional double heterostructure laser diodes. In addition to having lower threshold current, higher modulation efficiency, and a circular beam profile easy to couple into optical fibers, they offer the advantages of parallel and cost-effective fabrication, testing and packaging, as well as the possibility of being densely packed in 1D and 2D arrays. To date, their broad application field extends from data communication to sensing. Moreover, true single-mode emission (a single longitudinal and transverse mode) is highly desirable for numerous applications such as spectroscopy, positioning, laser printing, and short-distance optical interconnects. Although VCSELs inherently lase in a single longitudinal mode due to their short cavity length, they tend to emit multiple transverse modes whose properties are defined by the lateral geometry of the laser and the complex interplay between thermal lensing, spatial hole-burning, self-focusing, and nonuniform current injection. Hence, comprehensive electrothermo-optical simulators are becoming essential tools to explore the design parameter space for an optimum solution and to minimize the critical cost factor and the time required for a design cycle.

This article deals with the design and implementation of a self-consistent 2D electrothermo-optical simulator for VCSELs [1]. The approach is to be considered in the context of the electrothermo-optical device simulator presented in [2] for the isothermal case and extended in [3] to include self-heating of the device. The method used to compute the optical modes of the VCSEL was presented in [4]. To explore and develop novel and diverse VCSEL device concepts, a versatile finite- element formulation of the electrothermo-optical problem is a suitable and computationally feasible approach.

Simulation Details

The device and circuit simulator DESSIS™ is used to solve the electrothermal equations. The electrothermal system of equations is discretized into rotationally symmetric 2D finite elements by the box method. The nonlinear set of equations obtained in this way is solved using a Newton–Raphson scheme. The typical number of finite elements is about 10 000 resulting in equation systems of the order of 70 000.

In principle, 3D finite elements could be used to compute rotationally nonsymmetric devices. However, in this work, a 2D formulation of the cross section perpendicular to the wafer surface (see Figure 1) was chosen. Using a body of revolution (BOR) expansion, the two lowest order linearly polarized fundamental LP01 (HE11) and first-order LP11 (TE01 + TM01 + HE21) can be obtained immediately.

The VCSEL distributed Bragg reflector (DBR) stacks are represented as homogeneous regions with effective material parameters for the electrical model. In contrast, the DBR stacks can be resolved for the optical problem. Consequently, two separate meshes are used: a coarse one (~10 000 finite elements) for the electrothermal problem and a finer one (~200 000 finite elements) for the optical problem. Linear interpolation translates variables between the two meshes.

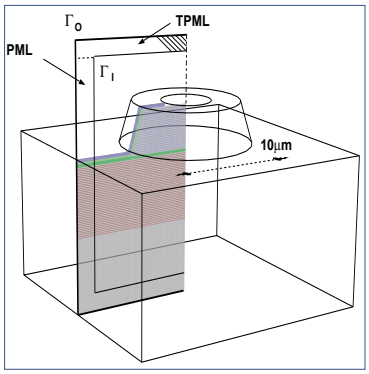


Figure 1: VCSEL device structure for simulation; the schematic separation of calculation domains relates to optical simulations with finite-element method (PML = perfectly matched layer); top PML (TPML) region is used to determine optical power emitted through the aperture of VCSEL

The resolution of the discretization for the two meshes is chosen such that spatial information in distributed quantities is preserved. The spontaneous and stimulated emission rates are restricted to the active region of the VCSEL. Therefore, the coarser electrothermal mesh only must be capable of resolving the optical field in the active region.

Optimization

The VCSEL device simulator was used to simulate a realistic 850 nm single-mode VCSEL device produced by Avalon Photonics Ltd. The device investigated is an oxide-confined device with an active diameter smaller than 4 µm to ensure single transverse mode operation. The epitaxial layer structure was grown on a GaAs wafer by metal-organic vapor-phase epitaxy (MOVPE) and designed for emission at 850 nm. The bottom DBR consists of 33 periods of alternating quarter-wave layers of $Al_{0.9}Ga_{0.1}As$ and $Al_{0.2}Ga_{0.8}As$. The one-lambda cavity consists of three GaAs quantum wells separated by $Al_{0.3}Ga_{0.7}As$ barriers and surrounded by the same material. The top DBR is made of 25 periods of $Al_{0.9}Ga_{0.1}As$ and $Al_{0.2}Ga_{0.8}As$ alternating quarter-wave layers. The whole layer stack is doped so as to form a p-i-n diode contacted between the top of the mesa and the rear side of the wafer. To confine the optical field and current, an oxidation layer is placed in the top DBR close to the cavity and at a minimum of the optical field. At room temperature, the MQW emission wavelength is 847.4 nm and the wavelength of the fundamental HE11 cavity mode is 840.7 nm. The two wavelengths coincide at a temperature of about 273 K. The cavity mode shifts by 0.06 nm/K, whereas the MQW emission shifts by 0.3 nm/K. The VCSEL achieves single-mode operation by a narrow oxide confinement that causes additional diffractive losses.

The optical model employed here accurately renders this effect. The electrothermal and optical equations are solved self-consistently and take into account the fundamental HE11

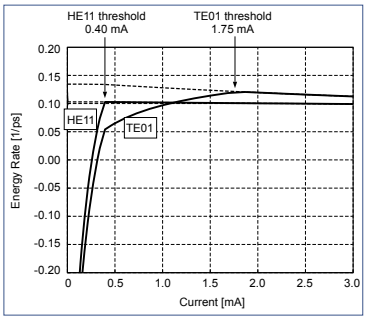


Figure 2: Simulation of modal gain (solid lines) and loss (dashed lines) of fundamental and first-order optical modes

and first-order TE01 modes. Figure 2 shows the evolution of the HE11 and TE01 modal gain and loss with respect to laser current. The modal loss of the TE01 mode decreases with increasing current because the evolving thermal lens pulls the mode towards the symmetry axis of the VCSEL. Consequently, less power is absorbed in the annular top metal contact. It follows that a comprehensive self-consistently coupled model such as that presented can only reproduce the correct threshold current for the first-order mode.

In Figures 3 and 4, excellent agreements between the simulated and measured DC terminal current, voltage, and wavelength characteristics are demonstrated over the specified operation range of the VCSEL. The simulation reproduces the threshold of the HE11 and TE01 modes at 0.40 mA and 1.75 mA, respectively. The change in wavelength is due to the thermally induced change in the refractive index of the resonator material. The characteristic mode splitting is clearly visible and indicates valid thermal modeling of the VCSEL structure.

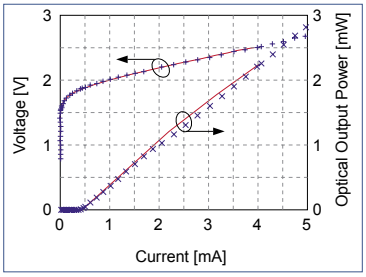


Figure 3: DC optical power and terminal voltage versus terminal current characteristics: simulation (crosses) and measurement (solid lines) are compared

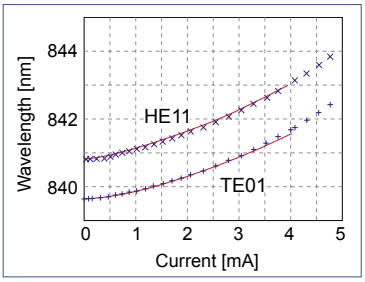


Figure 4: Wavelength tuning of fundamental and first-order optical mode: simulation (crosses) and measurement (solid lines) are compared

The oxide confinement leads to current crowding at the edge of the aperture and to a concentration of the current above the MQW region (see Figure 5). This results in increased Joule heating and the formation of a thermal lens at the center of the device. Furthermore, the high optical field intensity on the symmetry axis of the device causes strong spatial hole-burning in the local optical material gain (see Figure 6).

The electrothermal model takes the first mirror pair of the DBR stacks on either side of the lambda cavity into account to model correctly the carrier injection into the cladding region. A homogeneous region using effective carrier mobility represents the remaining portion of the DBR stacks.

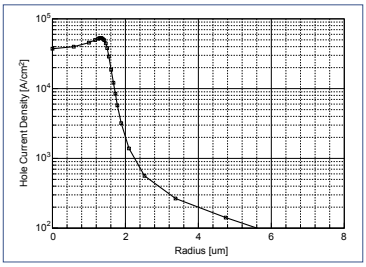


Figure 5: Hole current density above active region at 4 mA

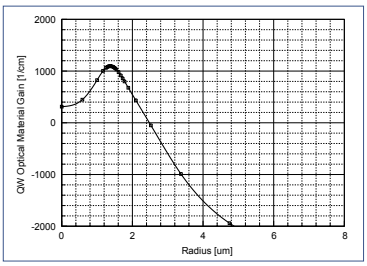


Figure 6: Local optical material gain at 4 mA

To calibrate the simulation, the real parts of the refractive indices n were obtained from Avalon Photonics Ltd and the relative changes with temperature are taken from the literature. Intermediate values are computed by linear interpolation. The imaginary part k is a fitting parameter and is set to the given value only in the extrinsic regions of the DBR stacks. It is set to zero in the intrinsic region of the laser diode.

Band-gap shrinkage due to temperature is only accounted for in the QW regions. The QW electron and hole mobilities are set equal to the bulk carrier mobilities in GaAs. The imaginary part of the complex refractive index, the SRH, Auger recombination parameters, and the DBR electron and hole mobilities were used to match simulated and measured results in Figures 3 and 4. The VCSEL structure is discretized with 14 526 finite elements for the electrothermal mesh and 93 545 finite elements for the optical mesh. The presented multimode computation requires 4.5 GB of memory. Calculating the 60 bias points shown in Figure 3 on a Compaq AlphaServer ES45 1250 MHz, using one processor, takes about 2.5 hours if the optical problem is only solved once at the beginning. If the optical problem is solved self-consistently, the same simulation takes about 9 hours. In this case, about 200 Newton optical mode solve steps must be performed. On average, a Newton step takes about 2 minutes and an optical solve step, about 30 seconds. The latter takes usually less time than stated due to the continuation scheme and the preconditioner recycling employed.

Conclusions

The model of a self-consistent 2D electrothermo-optical device simulator for VCSEL devices and its implementation in a software simulator were presented. The model is based on the photon rate equation approach. It was shown how the generic frequency domain finite-element formulation of the VCSEL optical problem fits into the context of electrothermo-optical VCSEL simulation. It was shown how the photon rate equation can be integrated into the Newton–Raphson scheme used to solve the system of electrothermal device equations. The latter significantly enhances the convergence properties of the simulator. The practical relevance of the implemented simulator was demonstrated with the accurate simulation of a realistic 850 nm single-mode VCSEL device produced by Avalon Photonics Ltd. In conclusion, the simulator DESSIS has an exceptionally advanced solver for the optical field, capable of predicting the cavity loss and the resonance wavelength to a high accuracy. It is a very versatile tool that, in comparison with an exclusive experimental procedure, allows considerable reduction of development costs and development time.

References

[1] M. Streiff et al., "A Comprehensive VCSEL Device Simulator," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 9, no. 3, pp. 879–891, 2003.

[2] B. Witzigmann, A. Witzig, and W. Fichtner, "A multidimensional laser simulation for edge-emitters including quantum carrier capture," *IEEE Transactions on Electron Devices*, vol. 47, no. 10, pp. 1926–1934, 2000.

[3] M. Pfeiffer, A. Witzig, and W. Fichtner, "Coupled electro-thermo-optical 3D simulation of edge-emitting lasers," *International Workshop on Numerical Simulation of Semiconductor Optoelectronic Devices*, University of California, Santa Barbara, 2001.

[4] M. Streiff, A. Witzig, and W. Fichtner, "Computing optical modes for VCSEL device simulation," *IEEE Proceedings Optoelectronics*, vol. 149, no. 4, pp. 166-173, 2002.

Tecplot in Disguise

ISE TCAD™ Release 10.0 will present ISE's Tecplot®-based visualization tool with a radically new and updated look. The main menu system as well as the traditional Tecplot sidebar have been replaced by ISE designs. The new design is a first, strong response to those users who asked for a simpler, more intuitive user interface, which is more specifically tailored to TCAD.

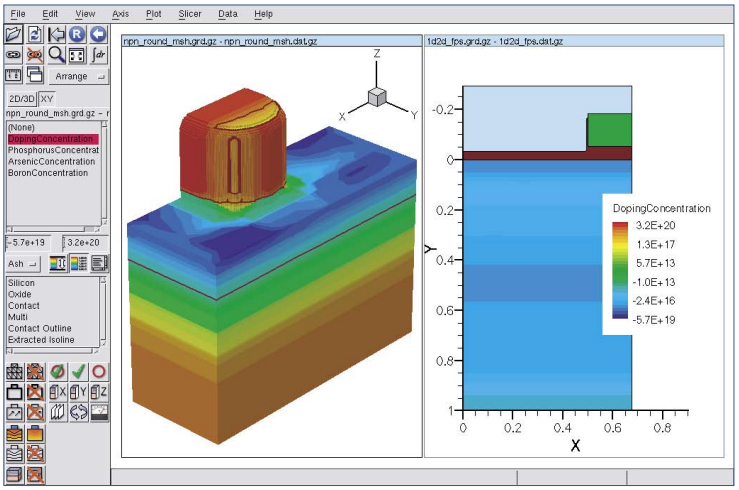
The new sidebar contains all the elements of the former TCAD tools panel in combination with frequently used elements from Tecplot's traditional sidebar. Most striking are the clear and colorful buttons, which make the interface more intuitive and help users to work more efficiently. The redesign of the menu system aims at positioning Tecplot's abundant and powerful functionality into a TCAD perspective. Compared with Tecplot's original menu system, the new one contains about 20% fewer entries.

While the new design will be certainly more attractive for the majority of the ISE TCAD users, some experienced users may prefer the traditional user interface to have full access to all Tecplot features. This is possible by specifying the command-line option `-ise:native`. While working with the new interface, it is also possible to switch between the traditional sidebar and the new ISE TCAD sidebar.

ISE will continue its efforts to optimize the user interface. A strong focus for the near future is to reduce the complexity of user interaction for specific tasks. ISE welcomes user feedback in this regard.

For more information about Tecplot, visit www.tecplot.com.

(Tecplot is a registered trademark of Tecplot Inc., Bellevue, WA, U.S.A.)



Tecplot-ISE with its new TCAD look

CMOS Image Sensor Simulations

CMOS image sensors (CISs) using 'standard' CMOS technologies are competing increasingly with charge-coupled device (CCD) image sensors. CISs have many advantages compared with CCDs: CISs consume less power than CCDs, all control circuits can be integrated onto the chip, and the manufacturing costs are lower for CISs compared to CCDs. These are the main reasons why CISs are so popular for cellular phone cameras.

Figure 1 depicts the circuit of a typical CIS: light is absorbed in the photodiode where it generates charge. The floating diffusion is set to 2 V by the Reset transistor. After the Reset transistor switches off, the Readout transistor is switched on, and the electrons collected in the photodiode flow to the floating diffusion and decrease the potential. The potential drop of the floating diffusion is amplified by the third transistor (Amp) and can be sensed by some circuitry outside the pixel array.

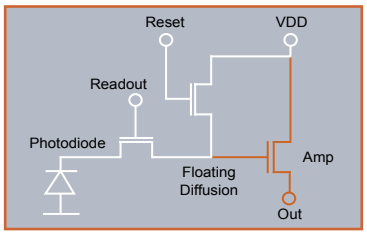


Figure 1: Circuit of CIS pixel; orange part was neglected in device simulation

Some device simulations of a CIS pixel are presented here. Figure 2 shows the structure of a typical CIS pixel. A lens on top of the oxide passivation layer focuses light onto a photodiode in the center of the pixel, where the light is absorbed and electron–hole pairs are generated. During readout, the transfer gate opens and the electrons generated in the photodiode flow into the floating diffusion and change the potential there. The second polygate visible in Figure 2 belongs to the Reset transistor, which separates V_{dd} from the floating diffusion.

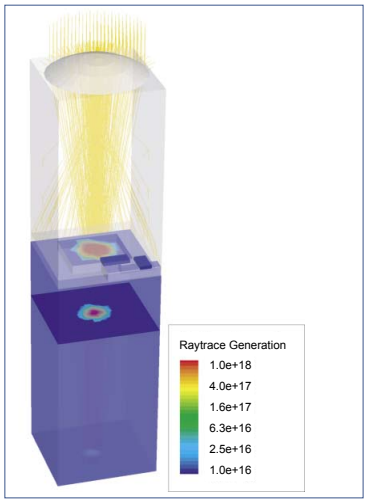


Figure 2: Carrier generation in a CIS pixel; light propagation through the lens onto the photodiode was simulated by 3D raytracing

Figure 3 compares the transient behavior of the floating diffusion voltage with and without illumination. In the first case, the wavelength was 600 nm and the wave power, 0.1 mW/cm^2. Readout and Reset were driven in the following way: during the first microsecond, the Reset transistor was switched on and the floating diffusion was set to 2 V. After one millisecond, the Reset transistor was switched off and the Readout transistor was opened and remained open until the end of the simulation. When the pixel was illuminated, the generated electrons flowed into the floating diffusion and decreased the potential. The velocity of the floating diffusion drop depends on the generated charge, the capacities of the photodiode and floating diode, and the switching characteristics of the Readout transistor.

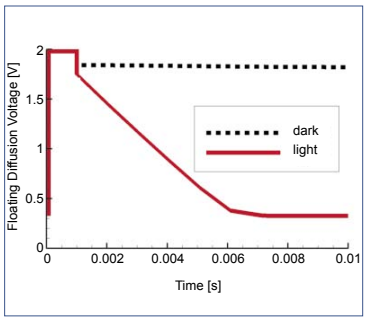


Figure 3: Floating diffusion voltage drop during illumination of pixel with a wavelength of 600 nm and a power of 0.1 mW/cm^2 compared with pixel not illuminated (dark)

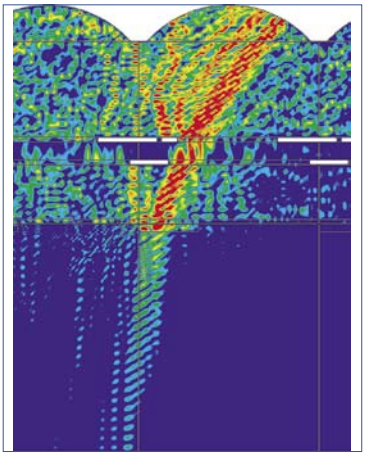


Figure 4: EMLAB full-wave simulation of optical crosstalk between neighboring pixel cells

One problem in the design of CISs is the optical and electrical noise that deteriorates the quality of the images. A main source of the noise is the optical crosstalk, which increases with decreasing pixel size. Optical crosstalk is best simulated with ISE's Maxwell equations solver EMLAB™. Figure 4 shows the propagation of an electromagnetic wave that hits the lens of the middle pixel coming from the upper-right corner. The simulation shows that the wave is partially focused on the photodiode of the middle pixel. However, due to diffraction at the metallization layers and reflection at the various material interfaces, optical noise is also coupled into the neighboring cells.

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ISE Integrated Systems Engineering AG
Affolternstrasse 52
CH-8050 Zurich
Switzerland

Phone: +41 44 389 9700
Fax: +41 44 389 9797
www.ise.ch

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